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1 Scope

The DCIM CPU Profile describes the properties and interfaces for executing system management tasks related to the management of processors within a system. The profile standardizes and aggregates the description for the CPU properties into a CPU view representation as well as provides static methodology for the clients to query the CPU views without substantial traversal of the model.

2 Normative References

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

DMTF DSP1033, Profile Registration Profile 1.0.0


Dell WSMAN Licenses and Privileges 1.0

DMTF DSP0226, Web Services for Management (WS-Management) Specification 1.1.0

DMTF DSP0227, WS-Management CIM Binding Specification 1.0.0

Dell Tech Center MOF Library http://www.delltechcenter.com/page/DCIM.Library.MOF

- DCIM_CPUView.mof
- DCIM_LCEnumeration.mof
- DCIM_LCRegisteredProfile.mof

3 Terms and Definitions

For the purposes of this document, the following terms and definitions apply.

3.1 conditional indicates requirements to be followed strictly in order to conform to the document when the specified conditions are met

3.2 mandatory indicates requirements to be followed strictly in order to conform to the document and from which no deviation is permitted
3.3
may
indicates a course of action permissible within the limits of the document

3.4
optional
indicates a course of action permissible within the limits of the document

3.5
referencing profile
indicates a profile that owns the definition of this class and can include a reference to this profile in its “Related Profiles” table

3.6
shall
indicates requirements to be followed strictly in order to conform to the document and from which no deviation is permitted

3.7
FQDD
Fully Qualified Device Descriptor is used to identify a particular component in a system.

3.8
Interop Namespace
Interop Namespace is where instrumentation instantiates classes to advertise its capabilities for client discovery.

3.9
Implementation Namespace
Implementation Namespace is where instrumentation instantiates classes relevant to executing core management tasks.

3.10
ENUMERATE
Refers to WS-MAN ENUMERATE operation as described in Section 8.2 of DSP0226_V1.1 and Section 9.1 of DSP0227_V1.0

3.11
GET
Refers to WS-MAN GET operation as defined in Section 7.3 of DSP00226_V1.1 and Section 7.1 of DSP0227_V1.0

4 Symbols and Abbreviated Terms

4.1
CIM
Common Information Model
4.2
iDRAC
Integrated Dell Remote Access Controller – management controller for blades and monolithic servers

4.3
CMC
Chassis Manager Controller – management controller for the modular chassis

4.4
WBEM
Web-Based Enterprise Management

5 Synopsis
Profile Name: CPU
Version: 1.1.0
Organization: Dell
CIM Schema Version: 2.26 Experimental
Dell Schema Version: 1.0.0
Interop Namespace: root/interop
Implementation Namespace: root/dcim
Central Class: DCIM_CPUView
Scoping Class: DCIM_ComputerSystem

The Dell CPU Profile is a component profile that contains the Dell specific implementation requirements for CPU view.

DCIM_CPUView shall be the Central Class.

Table 1 identifies profiles that are related to this profile.

<table>
<thead>
<tr>
<th>Profile Name</th>
<th>Organization</th>
<th>Version</th>
<th>Relationship</th>
</tr>
</thead>
<tbody>
<tr>
<td>Profile Registration</td>
<td>DCIM</td>
<td>1.0</td>
<td>Reference</td>
</tr>
</tbody>
</table>
6 Description

The Dell CPU Profile describes platform’s CPUs. Each CPU’s information is represented by an instance of DCIM_CPUView class.

Figure 1 details the class diagram of the Dell CPU Profile.

![Class Diagram]

**Figure 1 – Class Diagram**
Figure 2 details typical Dell CPU Profile implementation for a platform containing two CPUs. In order for client to discover the instrumentation’s support of this profile, CPUProfile is instantiated in the Interop Namespace. CPUProfile instance describes the information about the implemented profile: most importantly, the name and version of the profile and the organization name that produced the profile.

CPU1 and CPU2 are the CPU views representing the two CPUs in the Implementation Namespace. They are associated to the Interop namespace’s CPUProfile instance.

---

**Figure 2 – CPU Profile Implementation**
7 Implementation Description

This section describes the requirements and guidelines for implementing Dell CPU Profile.

Table 2 – Class Requirements: CPU Profile

<table>
<thead>
<tr>
<th>Element Name</th>
<th>Requirement</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Classes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DCIM_CPUView</td>
<td>Mandatory</td>
<td>The class shall be implemented in the Implementation Namespace. See section 7.1.</td>
</tr>
<tr>
<td>DCIM_LCElementConformsToProfile</td>
<td>Mandatory</td>
<td>The class shall be implemented in the Implementation Namespace.</td>
</tr>
<tr>
<td>DCIM_LCElementConformsToProfile</td>
<td>Mandatory</td>
<td>The class shall be implemented in the Interop Namespace.</td>
</tr>
<tr>
<td>DCIM_LCRegisteredProfile</td>
<td>Mandatory</td>
<td>The class shall be implemented in the Interop Namespace. See section 7.2.</td>
</tr>
<tr>
<td>Indications</td>
<td></td>
<td></td>
</tr>
<tr>
<td>None defined in this profile</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

7.1 CPU View – DCIM_CPUView

This section describes the implementation for the DCIM_CPUView class.

This class shall be instantiated in the Implementation Namespace.

The DCIM_LCElementConformsToProfile association(s) shall reference the DCIM_CPUView instance(s).

7.1.1 Resource URIs for WinRM®

The class Resource URI shall be “http://schemas.dell.com/wbem/wscim/1/cim-schema/2/DCIM_CPUView?__cimnamespace=root/dcim”

The key property shall be the InstanceID.


7.1.2 Operations

The following table details the implemented operations on DCIM_CPUView.

Table 3 – DCIM_CPUView - Operations

<table>
<thead>
<tr>
<th>Operation Name</th>
<th>Requirements</th>
<th>Required Input</th>
</tr>
</thead>
<tbody>
<tr>
<td>Get</td>
<td>Mandatory</td>
<td>Instance URI</td>
</tr>
<tr>
<td>Enumerate</td>
<td>Mandatory</td>
<td>Class URI</td>
</tr>
</tbody>
</table>
### 7.1.3 Properties

The following table details the implemented properties for DCIM_CPUView instance representing a processor in a system. The “Requirements” column shall denote the implementation requirement for the corresponding property. If the column “Property Name” matches the property name, the property either shall have the value denoted in the corresponding column “Additional Requirement”, or shall be implemented according to the requirements in the corresponding column “Additional Requirement”.

**Table 4 – DCIM_CPUView - Properties**

<table>
<thead>
<tr>
<th>Property Name</th>
<th>Requirements</th>
<th>Type</th>
<th>Requirement and Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cache1Associativity</td>
<td>Mandatory</td>
<td>uint16</td>
<td>An integer enumeration defining the system cache associativity:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&quot;1&quot; - &quot;Unknown&quot;, &quot;2&quot; - &quot;Other&quot;, &quot;3&quot; - &quot;Direct Mapped&quot;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&quot;4&quot; - &quot;2-way Set-Associative&quot;, &quot;5&quot; - &quot;4-way Set-Associative&quot;, &quot;6&quot; - &quot;Fully Associative&quot;,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&quot;7&quot; - &quot;8-way Set-Associative&quot;, &quot;8&quot; - &quot;16-way Set-Associative&quot;, &quot;9&quot; - &quot;12-way Set-Associative&quot;,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&quot;10&quot; - &quot;24-way Set-Associative&quot;, &quot;11&quot; - &quot;32-way Set-Associative&quot;, &quot;12&quot; - &quot;48-way Set-Associative&quot;,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&quot;13&quot; - &quot;64-way Set-Associative&quot;, &quot;14&quot; - &quot;20-way Set-Associative&quot;</td>
</tr>
<tr>
<td>Cache1ErrorMethodology</td>
<td>Optional</td>
<td>uint16</td>
<td>Cache ErrorMethodology - Contains the enumerated value that describes the cache’s error detection/correction mechanism</td>
</tr>
<tr>
<td>Cache1Level</td>
<td>Mandatory</td>
<td>uint16</td>
<td>The cache level for Cache1 labeled cache.</td>
</tr>
<tr>
<td>Cache1PrimaryStatus</td>
<td>Mandatory</td>
<td>uint32</td>
<td>Cache1PrimaryStatus provides a high level status value, intended to align with Red-Yellow-Green type representation of status.</td>
</tr>
<tr>
<td>Cache1Size</td>
<td>Mandatory</td>
<td>uint64</td>
<td>The property shall represent the total memory size of the cache in KBytes.</td>
</tr>
<tr>
<td>Cache1SRAMType</td>
<td>Mandatory</td>
<td>uint16</td>
<td>Cache SRAM Type.</td>
</tr>
<tr>
<td>Cache1Type</td>
<td>Mandatory</td>
<td>uint16</td>
<td>Defines whether this is for instruction caching (value=3), data caching (value=4) or both (value=5, &quot;Unified&quot;). Also, &quot;Other&quot; (1) and &quot;Unknown&quot; (2) can be defined.</td>
</tr>
<tr>
<td>Cache1WritePolicy</td>
<td>Mandatory</td>
<td>uint16</td>
<td>Defines whether this is write-back (value=1) or write-through (value=0) Cache, or whether this information &quot;Varies with Address&quot; (2) or &quot;Unknown&quot; (3) can be specified.</td>
</tr>
<tr>
<td>Cache1Location</td>
<td>Mandatory</td>
<td>uint8</td>
<td>Specifies the location of cache</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0- Internal</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1- External</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2- Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3- Unknown</td>
</tr>
<tr>
<td>Cache2Associativity</td>
<td>Mandatory</td>
<td>uint16</td>
<td>An integer enumeration defining the system cache associativity:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&quot;1&quot; - &quot;Unknown&quot;, &quot;2&quot; - &quot;Other&quot;, &quot;3&quot; - &quot;Direct Mapped&quot;</td>
</tr>
<tr>
<td>Property Name</td>
<td>Requirements</td>
<td>Type</td>
<td>Requirement and Description</td>
</tr>
<tr>
<td>----------------</td>
<td>--------------</td>
<td>------</td>
<td>----------------------------</td>
</tr>
<tr>
<td>Cache2ErrorMethodology</td>
<td>Optional</td>
<td>uint16</td>
<td>Cache ErrorMethodology - Contains the enumerated value that describes the cache's error detection/correction mechanism</td>
</tr>
<tr>
<td>Cache2Level</td>
<td>Mandatory</td>
<td>uint16</td>
<td>The cache level for Cache2 labeled cache.</td>
</tr>
<tr>
<td>Cache2PrimaryStatus</td>
<td>Mandatory</td>
<td>uint32</td>
<td>Cache2PrimaryStatus provides a high level status value, intended to align with Red-Yellow-Green type representation of status.</td>
</tr>
<tr>
<td>Cache2Size</td>
<td>Mandatory</td>
<td>uint64</td>
<td>The property shall represent the total memory size of the cache in KBytes.</td>
</tr>
<tr>
<td>Cache2SRAMType</td>
<td>Mandatory</td>
<td>uint16</td>
<td>Cache SRAM Type.</td>
</tr>
<tr>
<td>Cache2Type</td>
<td>Mandatory</td>
<td>uint16</td>
<td>Defines whether this is for instruction caching (value=3), data caching (value=4) or both (value=5, &quot;Unified&quot;). Also, &quot;Other&quot; (1) and &quot;Unknown&quot; (2) can be defined.</td>
</tr>
<tr>
<td>Cache2WritePolicy</td>
<td>Mandatory</td>
<td>uint16</td>
<td>Specifies the location of cache</td>
</tr>
<tr>
<td>Cache2Location</td>
<td>Mandatory</td>
<td>uint8</td>
<td>0 - Internal</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 - External</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2 - Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3 - Unknown</td>
</tr>
<tr>
<td>Cache3Associativity</td>
<td>Mandatory</td>
<td>uint16</td>
<td>An integer enumeration defining the system cache associativity: &quot;1&quot; - &quot;Unknown&quot;, &quot;2&quot; - &quot;Other&quot;, &quot;3&quot; - &quot;Direct Mapped&quot;</td>
</tr>
<tr>
<td>Cache3ErrorMethodology</td>
<td>Optional</td>
<td>uint16</td>
<td>Cache ErrorMethodology - Contains the enumerated value that describes the cache's error detection/correction mechanism</td>
</tr>
<tr>
<td>Cache3Level</td>
<td>Mandatory</td>
<td>uint16</td>
<td>The cache level for Cache3 labeled cache.</td>
</tr>
<tr>
<td>Property Name</td>
<td>Requirements</td>
<td>Type</td>
<td>Requirement and Description</td>
</tr>
<tr>
<td>---------------------------</td>
<td>--------------</td>
<td>---------</td>
<td>---------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Cache3PrimaryStatus</td>
<td>Mandatory</td>
<td>uint32</td>
<td>Cache3PrimaryStatus provides a high level status value, intended to align with Red-Yellow-Green type representation of status.</td>
</tr>
<tr>
<td>Cache3Size</td>
<td>Mandatory</td>
<td>uint64</td>
<td>The property shall represent the total memory size of the cache in KBytes.</td>
</tr>
<tr>
<td>Cache3SRAMType</td>
<td>Mandatory</td>
<td>uint16</td>
<td>Cache SRAM Type.</td>
</tr>
<tr>
<td>Cache3Type</td>
<td>Mandatory</td>
<td>uint16</td>
<td>Defines whether this is for instruction caching (value=3), data caching (value=4) or both (value=5, &quot;Unified&quot;). Also, &quot;Other&quot; (1) and &quot;Unknown&quot; (2) can be defined.</td>
</tr>
<tr>
<td>Cache3WritePolicy</td>
<td>Mandatory</td>
<td>uint16</td>
<td>Specifies the location of cache</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0- Internal</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1- External</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2- Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3- Unknown</td>
</tr>
<tr>
<td>Cache3Location</td>
<td>Mandatory</td>
<td>uint8</td>
<td>The characteristics include certain features of the processor such as 64 bit support for data width of the processor.</td>
</tr>
<tr>
<td>Characteristics</td>
<td>Mandatory</td>
<td>uint32</td>
<td>The characteristics include certain features of the processor such as 64 bit support for data width of the processor.</td>
</tr>
<tr>
<td>CPUFamily</td>
<td>Mandatory</td>
<td>string</td>
<td>The property shall represent processor family type in hexadecimals.</td>
</tr>
<tr>
<td>CPUStatus</td>
<td>Mandatory</td>
<td>uint16</td>
<td>Indicates the current status of the Processor. For example, the Processor might be disabled due to a POST error (value=3).</td>
</tr>
<tr>
<td>CurrentClockSpeed</td>
<td>Mandatory</td>
<td>uint32</td>
<td>The property value shall be in MHz. The current speed (in MHz) of this Processor.</td>
</tr>
<tr>
<td>ExternalBusClockSpeed</td>
<td>Mandatory</td>
<td>uint32</td>
<td>The property value shall be in MHz. The speed (in MHz) of the external bus interface (known as the front side bus).</td>
</tr>
<tr>
<td>FQDD</td>
<td>Mandatory</td>
<td>string</td>
<td>A string containing the Fully Qualified Device Description, a user-friendly name for the object.</td>
</tr>
<tr>
<td>InstanceID</td>
<td>Mandatory</td>
<td>string</td>
<td>The property value shall be the FQDD property value.</td>
</tr>
<tr>
<td>DeviceDescription</td>
<td>Mandatory</td>
<td>string</td>
<td>A string containing the friendly Fully Qualified Device Description, a property that describes the device and its location</td>
</tr>
<tr>
<td>Manufacturer</td>
<td>Mandatory</td>
<td>string</td>
<td>The name of the organization responsible for producing the processor.</td>
</tr>
<tr>
<td>MaxClockSpeed</td>
<td>Mandatory</td>
<td>uint32</td>
<td>The property value shall be in MHz. The maximum speed (in MHz) of this Processor.</td>
</tr>
<tr>
<td>Model</td>
<td>Mandatory</td>
<td>string</td>
<td>The make and or model of the product</td>
</tr>
<tr>
<td>NumberofEnabledCores</td>
<td>Mandatory</td>
<td>uint32</td>
<td>Number of processor cores enabled for processor.</td>
</tr>
<tr>
<td>NumberofEnabledThreads</td>
<td>Mandatory</td>
<td>uint32</td>
<td>Total number of hardware enabled threads for processor.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>NOTE: The disabling of the multithreading by the BIOS does not affect the number of hardware enabled threads reported by this property.</td>
</tr>
</tbody>
</table>
### Property Name | Requirements | Type   | Requirement and Description
---|---|---|---
NumberOfProcessorCores | Mandatory | uint32 | Number of processor cores available for processor.
HyperThreadingEnabled | Mandatory | uint8 | 0-No 1-Yes
HyperThreadingCapable | Mandatory | uint8 | 0-No 1-Yes
VirtualizationTechnologyEnabled | Mandatory | uint8 | 0-No 1-Yes
VirtualizationTechnologyCapable | Mandatory | uint8 | 0-No 1-Yes
ExecuteDisabledEnabled | Mandatory | uint8 | 0-No 1-Yes
ExecuteDisabledCapable | Mandatory | uint8 | 0-No 1-Yes
TurboModeEnabled | Mandatory | uint8 | 0-No 1-Yes
TurboModeCapable | Mandatory | uint8 | 0-No 1-Yes
PrimaryStatus | Mandatory | uint32 | PrimaryStatus provides a high level status value, intended to align with Red-Yellow-Green type representation of status.
Voltage | Mandatory | string | The property shall represent the voltage(s) of the processor in Volts.
LastSystemInventoryTime | Mandatory | string | This property provides the last time \"System Inventory Collection On Reboot(CSIOR)\" was performed. The value is represented as yyyyMMddHHMMSS.
LastUpdateTime | Mandatory | string | This property provides the last time the data was updated. The value is represented as yyyyMMddHHMMSS

### 7.2 CPU Profile Profile Registration

This section describes the implementation for the DCIM_LCRegisteredProfile class.

This class shall be instantiated in the Interop Namespace.

The DCIM_LCElmentConformsToProfile association(s) shall reference the DCIM_LCRegisteredProfile instance.

#### 7.2.1 Resource URIs for WinRM®

The class Resource URI shall be “http://schemas.dmtf.org/wbem/wscim/1/cim-schema/2/CIM_RegisteredProfile?__cimnamespace=root/interop"

The key property shall be the InstanceID property.

The instance Resource URI shall be: “http://schemas.dell.com/wbem/wscim/1/cim-schema/2/DCIM_LCRegisteredProfile?__cimnamespace=root/interop+InstanceId=DCIM:CPU:1.0.0”

#### 7.2.2 Operations

The following table details the implemented operations on DCIM_LCRegisteredProfile.
7.2.3 Properties

The following table details the implemented properties for DCIM_LCRegisteredProfile instance representing CPU Profile implementation. The “Requirements” column shall denote the implementation requirement for the corresponding property. If the column “Name” matches the property name, the property either shall have the value denoted in the corresponding column “Additional Requirements”, or shall be implemented according to the requirements in the corresponding column “Additional Requirements”.

<table>
<thead>
<tr>
<th>Property Name</th>
<th>Requirement</th>
<th>Type</th>
<th>Additional Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>InstanceID</td>
<td>Mandatory</td>
<td>String</td>
<td>DCIM:CPU:1.0.0</td>
</tr>
<tr>
<td>RegisteredName</td>
<td>Mandatory</td>
<td>String</td>
<td>This property shall have a value of &quot;CPU&quot;.</td>
</tr>
<tr>
<td>RegisteredVersion</td>
<td>Mandatory</td>
<td>String</td>
<td>This property shall have a value of &quot;1.1.0&quot;.</td>
</tr>
<tr>
<td>RegisteredOrganization</td>
<td>Mandatory</td>
<td>Uint16</td>
<td>This property shall have a value of 1 (Other).</td>
</tr>
<tr>
<td>OtherRegisteredOrganization</td>
<td>Mandatory</td>
<td>String</td>
<td>The property value shall match “DCIM”.</td>
</tr>
<tr>
<td>AdvertisedTypes[]</td>
<td>Mandatory</td>
<td>Uint16</td>
<td>This property array shall contain [1(Other), 1 (Other)].</td>
</tr>
<tr>
<td>AdvertiseTypeDescriptions[]</td>
<td>Mandatory</td>
<td>String</td>
<td>This property array shall contain [&quot;WS-Identify&quot;, &quot;Interop Namespace&quot;].</td>
</tr>
<tr>
<td>ProfileRequireLicense[]</td>
<td>Mandatory</td>
<td>String</td>
<td>This property array shall describe the required licenses for this profile. If no license is required for the profile, the property shall have value NULL.</td>
</tr>
</tbody>
</table>
| ProfileRequireLicenseStatus[]  | Mandatory   | String   | This property array shall contain the status for the corresponding license in the same element index of the ProfileRequireLicense array property. Each array element shall contain: 
  - “LICENSED”
  - “NOT_LICENSED”
If no license is required for the profile, the property shall have value NULL. |

8 Methods

This section details the requirements for supporting extrinsic methods for the CIM elements defined by this profile.

No additional details specified.

9 Use Cases

See Lifecycle Controller (LC) Integration Best Practices Guide.
10 CIM Elements

No additional details specified.

11 Privilege and License Requirement

The following table describes the privilege and license requirements for the listed operations. For the detailed explanation of the privileges and licenses, refer to the Dell WSMAN Licenses and Privileges specification.

<table>
<thead>
<tr>
<th>Class and Method</th>
<th>Operation</th>
<th>User Privilege Required</th>
<th>License Required</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCIM_CPUView</td>
<td>ENUMERATE, GET</td>
<td>Login</td>
<td>LM_REMOTE_ASSET_INVENTORY</td>
</tr>
<tr>
<td>DCIM_LCElementConformsToProfile</td>
<td>ENUMERATE, GET</td>
<td>Login</td>
<td>None.</td>
</tr>
<tr>
<td>DCIM_LCRegisteredProfile</td>
<td>ENUMERATE, GET</td>
<td>Login</td>
<td>None.</td>
</tr>
</tbody>
</table>
### ANNEX A
(informative)

### Change Log

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
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