2nd Generation AMD EPYC™ Processors: Balanced Memory Reference Guide

Tech Note by

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Summary

Understanding how to configure balanced memory on a PowerEdge server running 2nd Generation AMD EPYC™ Processors is critical for securing high memory bandwidth and low memory access latency.

This tech note explains the required guidelines that must be obeyed to achieve balanced memory, as well as supporting tables and illustrations for visual clarity.

When DIMMs are populated in an unbalanced fashion, memory bandwidth can be significantly reduced from its maximum potential. PowerEdge customers seeking maximum memory bandwidth and minimized memory access latency should populate DIMMs in a balanced configuration, or a near balanced configuration if balanced cannot be implemented. Populating memory in accord with the guidelines in this technote will ensure optimized performance.

Guidelines for Balanced Memory

1. Balanced Configuration
   - **Populate all memory channels with one or two DIMMs for best performance;** a total of eight or sixteen DIMMs per CPU
2. Near Balanced Configuration
   - Populate four or twelve DIMMs per CPU
   - Populate DIMMs in correct assembly order (*see Figure 1*)
3. All CPU and DIMM parts must be identical
4. All server sockets should have identical memory configurations

Assembly Order

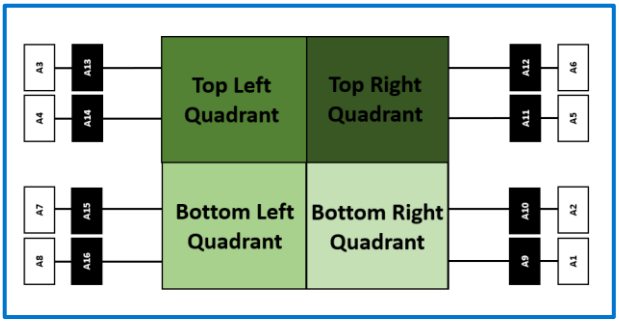

Figure 1: DIMM population order, starting with A1 and ending with A16

* If you are interested in reading the full white paper on balanced memory, please click here

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