# Statement of Volatility – Dell EMC PowerEdge R7425

Dell PowerEdge R7425 contains both volatile and non-volatile (NV) components.  Volatile components lose their data immediately upon removal of power from the component. Non-volatile components continue to retain their data even after the power has been removed from the component. Components chosen as user-definable configuration options (those not soldered to the motherboard) are not included in the Statement of Volatility. Configuration option information (pertinent to options such as microprocessors, remote access controllers, and storage controllers) is available by component separately.  The following NV components are present in the PowerEdge R7425 server.

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size |
|---|---|---|---|---|
| **Planer** | | | | |
| BIOS Password (part of CPU internal CMOS RAM) | Non-Volatile | 1 | U24 | 16 bytes (out of 256 bytes used for CPU Internal CMOS RAM) |
| Primary BIOS SPI Flash | Non-Volatile | 1 | U422 | 32 MB |
| iDRAC SPI Flash | Non-Volatile | 1 | U217 | 4 MB |
| BMC EMMC | Non-Volatile | 1 | U_EMMC1 | 4 GB |
| CPU VDDCR Regulators | Non-Volatile | 2 | U373, U383 | 2 KB |
| CPU VSOC Regulators | Non-Volatile | 2 | U380, U390 | 2 KB |
| CPU Vmem Regulators | Non-Volatile | 4 | U393, U398, U403, U408 | 2 KB |
| System CPLD RAM | Volatile | 1 | U_CPLD | 92Kb |
| System CPLD FLASH | Non-Volatile | 1 | U_CPLD | 256Kb |
| System Memory: RDIMM and LRDIMM | Volatile | Up to 16 per CPU | CPU<2:1>_CH<H:A>_D<1:0> | Up to 32GB per DIMM |
| Internal USB Key | Non-Volatile | Up to 1 | J_USB_INT | Varies (not factory installed) |
| CPU | Volatile | 1 or 2 | U24 / U15 | Various |
| iDRAC DDR | Volatile | 1 | U_IDRAC9_DRAM1 | 512Mb |
| iDRAC | Volatile | 1 | U_IDRAC | For CPU:  128KB + Registers |

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| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size |
|---|---|---|---|---|
| | | | | Co-proc: 64Kb + Registers |
| Recovery BIOS SPI | Non-Volatile | 1 | U208 | 16MB |
| **2x2.5" Rear Backplane** | | | | |
| SEP internal flash | Non-Volatile | 1 | U_SEP | Flash:64KB+4KB EEPROM: 2KB |
| Backplane External FRU | Non-Volatile | 1 | U_BP_EEPROM | 256 Bytes |
| **4x2.5" Mid NVMe Backplane** | | | | |
| SEP internal flash | Non-Volatile | 1 | U_SEP1 | Flash:64KB+4KB EEPROM: 2KB |
| **4x3.5" Mid Backplane** | | | | |
| SEP internal flash | Non-Volatile | 1 | U_SEP | Flash:32KB+4KB EEPROM: 1KB |
| Backplane External FRU | Non-Volatile | 1 | U_BP_EEPROM | 256 Bytes |
| **24x2.5" EXP/Backplane** | | | | |
| NVSRAM memory | Non-Volatile | 1 | U_NVSRAM | 1 Mb |
| Flash memory | Non-Volatile | 1 | U_FLASH | 128 Mb |
| Expander FRU | Non-Volatile | 1 | U_EXP_EEPROM | 512 Bytes |
| Backplane FRU | Non-Volatile | 1 | U_BP_EEPROM | 256 Bytes |
| **8x3.5" Backplane** | | | | |
| SEP internal flash | Non-Volatile | 1 | U_SEP | Flash:64KB+4KB EEPROM: 2KB |
| **12x3.5" EXP/Backplane** | | | | |
| NVSRAM memory | Non-Volatile | 1 | U_NVSRAM | 1 Mb |
| Flash memory | Non-Volatile | 1 | U_FLASH | 128 Mb |
| Backplane FRU | Non-Volatile | 1 | U_BP_FRU | 256 Bytes |
| Expander FRU | Non-Volatile | 1 | U_EXP_FRU | 512 Bytes |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size |
|---|---|---|---|---|
| **4x2.5" Rear Backplane** | | | | |
| SEP internal flash | Non-Volatile | 1 | U_SEP | Flash:64KB+4KB EEPROM: 2KB |
| Backplane FRU | Non-Volatile | 1 | U_BP_EEPROM | 256 Bytes |
| **24x2.5" NVME EXP** | | | | |
| PSoC | Non-Volatile | 1 | U_8 | 128 kB |
| Expander FRU image | Non-Volatile | 1 | U_FRU | 2Kb |
| **24x2.5" NVME BP** | | | | |
| SEP internal flash | Non-Volatile | 2 | U_SEP1, U_SEP2 | Flash:64KB+4KB EEPROM: 2KB |
| HOTPLUG_PERST BUFFER | Non-Volatile | 1 | U35, U42 | 16 KB |
| **H730P, H740P, H840 PERCs** | | | | |
| NVSRAM | Non-volatile | 1 | U1087 | 128KB |
| FRU | Non-volatile | 1 | U1019 | 256B |
| SPD | Non-volatile | 1 | U22 | 256B |
| Flash | Non-volatile | 1 | U1086 | 16MB |
| Backup Flash | Non-volatile | 1 | U1100 | 8GB |
| SDRAM | Volatile | 9 | U1077-U1085 | 8GB |
| **H330 PERC** | | | | |
| NVSRAM | Non-volatile | 1 | U1033 | 128KB |
| FRU | Non-volatile | 1 | U1019 | 256B |
| 1-Wire EEPROM | Non-volatile | 1 | U1004 | 128B |
| Serial Boot ROM | Non-volatile | 1 | U1020 | 8KB |
| Flash | Non-volatile | 1 | U3 | 16MB |
| **HBA330 PERC** | | | | |
| NVSRAM | Non-volatile | 1 | U1033 | 128KB |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size |
|------|--------------------------|----------|----------------------|------|
| FRU | Non-volatile | 1 | U1019 | 256B |
| Serial Boot ROM | Non-volatile | 1 | U1020 | 8KB |
| Flash | Non-volatile | 1 | U3 | 16MB |
| **Left Status Control Panel** | | | | |
| Microcontroller | Non-Volatile | 1 | U_TINY | 8KB |
| **Left Control Panel with Quick Sync 2** | | | | |
| Microcontroller | Non-Volatile | 1 | USAM7 | 32Mb |
| **TPM** | | | | |
| Trusted Platform Module (TPM) | Non-Volatile | 1 | U_TPM | 128 Bytes |
| **Right Control Panel** | | | | |
| SPI Flash | Non-Volatile | 1 | U2 | 32 Mb |
| **IDSDM - vFlash** | | | | |
| vFlash (uSD) | Non-Volatile | 1 | J3 | 16GB |
| iDSDM (uSD1, uSD2) | Non-Volatile | 2 | J1, J2 | 16GB, 32GB, 64GB |
| SPI Flash | Non-Volatile | 1 | U2 | 1MB |
| **BOSS** | | | | |
| SPI FLASH | Non-Volatile | 1 | U17 | 1024KB |
| TFRU | Non-Volatile | 1 | U7 | 64KB |
| **LCD Bezel** | | | | |
| Microcontroller | Non-Volatile | 1 | IC1 | 256KB |
| **PSU** | | | | |
| Microcontroller | Non-Volatile | Up to 3 | Microchip | Up to 64KB |

| Item | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) |
|---|---|---|---|
| **Planer** | | | |
| BIOS Password (part of CPU internal CMOS RAM) | Battery-backed CMOS RAM | Yes | Password to change BIOS settings |
| Primary BIOS SPI Flash | SPI Flash | No | Boot code |
| iDRAC SPI Flash | SPI Flash | No | iDRAC Uboot (bootloader) |
| BMC EMMC | eMMC NAND Flash | No | Operational iDRAC FW, Lifecycle Controller (LC) USC partition, LC service diags, LC OS drivers, USC firmware |
| CPU VDDCR Regulators | ROM | No | Operational parameters |
| CPU VSOC Regulators | ROM | No | Operational parameters |
| CPU Vmem Regulators | ROM | No | Operational parameters |
| System CPLD RAM | FLASH | No | Not utilized |
| System CPLD FLASH | RAM | No | Power on System Firmware |
| System Memory: RDIMM and LRDIMM | DRAM | Yes | System OS RAM |
| Internal USB Key | Flash | Yes | General purpose USB key drive |
| CPU | Cache + registers | Yes | Processor cache + registers |
| iDRAC DDR | DRAM | No | iDRAC local memory |
| iDRAC | Cache + registers | No | Processor cache + registers |
| Recovery BIOS SPI | SPI Flash | No | Recovery image |
| **2x2.5" Rear Backplane** | | | |
| SEP internal flash | Integrated Flash+EEPROM | No | Firmware + FRU |
| Backplane External FRU | I2C EEPROM | No | FRU |

| Item | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) |
|---|---|---|---|
| **4x2.5" Mid NVMe Backplane** | | | |
| SEP internal flash | Integrated Flash+EEPROM | No | Firmware + FRU |
| **4x3.5" Mid Backplane** | | | |
| SEP internal flash | Integrated Flash+EEPROM | No | Firmware + FRU |
| Backplane External FRU | I2C EEPROM | No | FRU |
| **24x2.5" EXP/Backplane** | | | |
| NVSRAM memory | Flash | No | FW config data |
| Flash memory | Flash | No | Firmware |
| Expander FRU | I2C EEPROM | No | FRU |
| Backplane FRU | I2C EEPROM | No | FRU |
| **8x3.5" Backplane** | | | |
| SEP internal flash | Integrated Flash+EEPROM | No | Firmware + FRU |
| **12x3.5" EXP/Backplane** | | | |
| NVSRAM memory | Flash | No | FW config data |
| Flash memory | Flash | No | Firmware |
| Backplane FRU | I2C EEPROM | No | FRU |
| Expander FRU | I2C EEPROM | No | FRU |
| **4x2.5" Rear Backplane** | | | |
| SEP internal flash | Integrated Flash+EEPROM | No | Firmware + FRU |
| Backplane  FRU | I2C EEPROM | No | FRU |
| **24x2.5" NVME EXP** | | | |
| PSoC | Flash | No | Configuration data |
| Expander FRU image | EEPROM | No | FRU |
| **24x2.5" NVME BP** | | | |
| SEP internal flash | Integrated Flash+EEPROM | No | Firmware + FRU |
| HOTPLUG_PERST BUFFER | FRAM | No | Configuration data |

| Item | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) |
|---|---|---|---|
| **H730P, H740P, H840 PERCs** | | | |
| NVSRAM | NVSRAM | No | Configuration data |
| FRU | FRU | No | Card manufacturing information |
| SPD | SPD | No | Memory configuration data |
| Flash | Flash | No | Card firmware |
| Backup Flash | Backup Flash | No | Holds cache data during power loss |
| SDRAM | SDRAM | No | Cache for HDD I/O |
| **H330 PERC** | | | |
| NVSRAM | NVSRAM | No | Configuration data |
| FRU | FRU | No | Card manufacturing information |
| 1-Wire EEPROM | 1-Wire EEPROM | No | Holds default controller properties/settings |
| Serial Boot ROM | Serial Boot ROM | No | Bootloader |
| Flash | Flash | No | Card firmware |
| **HBA330 PERC** | | | |
| NVSRAM | NVSRAM | No | Configuration data |
| FRU | FRU | No | Card manufacturing information |
| Serial Boot ROM | Serial Boot ROM | No | Bootloader |
| Flash | Flash | No | Card firmware |
| **Left Status Control Panel** | | | |
| Microcontroller | Flash | No | Driving Health and Status LED |
| **Left Control Panel with Quick Sync 2** | | | |
| Microcontroller | SPI Flash | No | For field maintenance. Have License, Service Tag and system information. Driving health and status LEDs |

| Item | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) |
|---|---|---|---|
| **TPM** | | | |
| Trusted Platform Module (TPM) | EEPROM | Yes | Storage of encryption keys |
| **Right Control Panel** | | | |
| SPI Flash | SPI Flash | No | EasyRestore functionality: contains Service Tag, Copy of SEL logs |
| **IDSDM - vFlash** | | | |
| vFlash (uSD) | NAND flash | Yes | populate out-of-band or optionally connect to the host as mass storage and boot mechanism |
| iDSDM (uSD1, uSD2) | NAND Flash | Yes | Provides mass storage |
| SPI Flash | SPI Flash | SPI flash is only indirectly connected to iDRAC. iDRAC can read any address in the SPI flash, but may only write the primary firmware storage area as a part of a firmware update procedure. | Boot firmware storage, configuration and state data for IDSDM. |
| **BOSS** | | | |
| SPI FLASH | FLASH EEPROM | No | Boot code, FW |
| TFRU | FLASH EEPROM | Yes | Thermal monitoring |
| **LCD Bezel** | | | |
| Microcontroller | Internal Flash | No | bootloader and s/w implementation of LCD command set |
| **PSU** | | | |
| Microcontroller | Flash PROM and EEPROM | Yes | Report PSU information and control firmware |

| Item | How is data input to this memory? | How is this memory write protected? |
|---|---|---|
| **Planer** | | |
| BIOS Password (part of CPU internal CMOS RAM) | Keyboard | N/A – BIOS only control |
| Primary BIOS SPI Flash | SPI interface via CPU | Software write protected |
| iDRAC SPI Flash | SPI interface via iDRAC | Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed. |
| BMC EMMC | NAND Flash interface via iDRAC | Embedded FW write protected |
| CPU VDDCR Regulators | Programmed at factory via I2C | No write protect |
| CPU VSOC Regulators | Programmed at factory via I2C | No write protect |
| CPU Vmem Regulators | Programmed at factory via I2C | No write protect |
| System CPLD RAM | Not utilized | Not accessible |
| System CPLD FLASH | Firmware update | BIOS Security Protocols |
| System Memory: RDIMM and LRDIMM | System OS | OS Control |
| Internal USB Key | USB interface via CPU. Accessed via system OS | No write protect |
| CPU | Various | Various |
| iDRAC DDR | iDRAC Firmware | No write protect |
| iDRAC | iDRAC Firmware | No write protect |
| Recovery BIOS SPI | SPI interface via iDRAC | No write protect |
| **2x2.5" Rear Backplane** | | |
| SEP internal flash | I2C interface via iDRAC | Program write protect bit |
| Backplane External FRU | Programmed at ICT during production. | No write protect |
| **4x2.5" Mid NVMe Backplane** | | |
| SEP internal flash | I2C interface via iDRAC | Program write protect bit |
| **4x3.5" Mid Backplane** | | |
| SEP internal flash | I2C interface via iDRAC | Program write protect bit |
| Backplane External FRU | Programmed at ICT during production. | No write protect |
| **24x2.5" EXP/Backplane** | | |

| Item | How is data input to this memory? | How is this memory write protected? |
|---|---|---|
| NVSRAM memory | Common Flash memory Interface (CFI) | Hardware strapping |
| Flash memory | Common Flash memory Interface (CFI) | Hardware strapping |
| Expander FRU | I2C interface via expander | Hardware strapping |
| Backplane FRU | I2C interface via iDRAC | Hardware strapping |
| **8x3.5" Backplane** | | |
| SEP internal flash | I2C interface via iDRAC | Program write protect bit |
| **12x3.5" EXP/Backplane** | | |
| NVSRAM memory | Common Flash memory Interface (CFI) | Hardware strapping |
| Flash memory | Common Flash memory Interface (CFI) | Hardware strapping |
| Backplane FRU | I2C interface via expander | Hardware strapping |
| Expander FRU | I2C interface via iDRAC | Hardware strapping |
| **4x2.5" Rear Backplane** | | |
| SEP internal flash | I2C interface via iDRAC | Program write protect bit |
| Backplane  FRU | Programmed at ICT during production. | No write protect |
| **24x2.5" NVME EXP** | | |
| PSoC | Pre-programmed before assembly. Can be updated using Dell/Cypress tools | Not WP. Not visible to Host Processor |
| Expander FRU image | Programmed at ICT during production. | Not WP |
| **24x2.5" NVME BP** | | |
| SEP internal flash | I2C interface via iDRAC | Program write protect bit |
| HOTPLUG_PERST BUFFER | Programmed at ICT during production. | Not WP |
| **H730P, H740P, H840 PERCs** | | |
| NVSRAM | ROC writes configuration data to NVSRAM | no write protect. Not visible to Host Processor |
| FRU | Programmed at ICT during production. | no write protect |

| Item | How is data input to this memory? | How is this memory write protected? |
|---|---|---|
| SPD | Pre-programmed before assembly | no write protect. Not visible to Host Processor |
| Flash | Pre-programmed before assembly. Can be updated using Dell/LSI tools | no write protect. Not visible to Host Processor |
| Backup Flash | FPGA backs up DDR data to this device in case of a power failure | no write protect. Not visible to Host Processor |
| SDRAM | ROC writes to this memory - using it as cache for data IO to HDDs | no write protect. Not visible to Host Processor |
| **H330 PERC** | | |
| NVSRAM | ROC writes configuration data to NVSRAM | no write protect. Not visible to Host Processor |
| FRU | Programmed at ICT during production | no write protect |
| 1-Wire EEPROM | ROC writes data to this memory | no write protect. Not visible to Host Processor |
| Serial Boot ROM | Pre-programmed before assembly | no write protect. Not visible to Host Processor |
| Flash | Pre-programmed before assembly. Can be updated using Dell/LSI tools | no write protect. Not visible to Host Processor |
| **HBA330 PERC** | | |
| NVSRAM | ROC writes configuration data to NVSRAM | no write protect. Not visible to Host Processor |
| FRU | Programmed at ICT during production | no write protect |
| Serial Boot ROM | Pre-programmed before assembly | no write protect. Not visible to Host Processor |
| Flash | Pre-programmed before assembly. Can be updated using Dell/LSI tools | no write protect. Not visible to Host Processor |
| **Left Status Control Panel** | | |
| Microcontroller | I2C via iDRAC | Hardware strapping |
| **Left Control Panel with Quick Sync 2** | | |
| Microcontroller | SPI interface via iDRAC | Hardware strapping |
| **TPM** | | |
| Trusted Platform Module (TPM) | Using TPM Enabled operating systems | SW write protected |

| Item | How is data input to this memory? | How is this memory write protected? |
|---|---|---|
| **Right Control Panel** | | |
| SPI Flash | SPI interface from iDRAC to Right Cntl Panel | Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed. |
| **IDSDM - vFlash** | | |
| vFlash (uSD) | User can provide data to iDRAC (entirely in the iDRAC domain) to be pushed into vFlash | no write protect |
| iDSDM (uSD1, uSD2) | device resides in host domain; they are exposed to the user via an internally connected, non-removable USB mass storage device | physical write protect switch on ACE card |
| SPI Flash | User can initiate a firmware update of the IDSDM device. | There is no mechanism provided to iDRAC to write any SPI NOR area outside of the primary IDSDM firmware region. |
| **BOSS** | | |
| SPI FLASH | By programming the image via firmware update process | N/A |
| TFRU | During Manufacturing, by programming the image via firmware update process.<br><br>During runtime, by I2C Proprietary Command Protocol | N/A |
| **LCD Bezel** | | |
| Microcontroller | Updated as part of secure iDRAC software update. Configuration parameters can change only as part of iDRAC update | Writes are only allowed as part of secure iDRAC update |
| **PSU** | | |
| Microcontroller | The data is flash via Dell Update Package(DUP) | Using signature and manufacture key to protect memory write |

**NOTE:** For any information that you may need, direct your questions to your Dell Marketing contact.