Statement of Volatility – Dell EMC PowerEdge– R6415

Dell EMC PowerEdge– R6415 contains both volatile and non-volatile (NV) components. Volatile components lose their data immediately upon removal of power from the component. Non-volatile components continue to retain their data even after the power has been removed from the component. Components chosen as user-definable configuration options (those not soldered to the motherboard) are not included in the Statement of Volatility. Configuration option information (pertinent to options such as microprocessors, remote access controllers, and storage controllers) is available by component separately. The following NV components are present in the PowerEdge– R6415 server.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
Planer				
CPU Internal CMOS RAM	Non-Volatile	1	CPU0	64M bytes
BIOS SPI Flash	Non-Volatile	1	U4	256 MB
iDRAC SPI Flash	Non-Volatile	1	U5	32 MB
BMC EMMC	Non-Volatile	1	U_EMMC2	8 GB
System CPLD RAM	Volatile	1	U_CPLD1	16 KB
System Memory	Volatile	1	CPU0: A1~A16,	Up to 32GB per DIMM (RDIMM) Up to 128GB per DIMM (LRDIMM)
Trusted Platform Module (TPM, TPM 2.0 only)	Non-Volatile	1	J_TPM_MODULE	128 Bytes
CPU Vcore and VDDCR SOC FW	Non-Volatile	1	PAAU1 PBAU1	16KB
MEM_VDDQ FW	Non-Volatile	1	PAEU1, PBEU1	16KB
LOM NVRAM	Non-Volatile	1	U_LOM1_ROM	1MB
Power Supplies				
Microcontroller	Non-Volatile	1	Microchip	Up to 64KB
1U 4x3.5” Backplane				
SEP internal flash	Non-Volatile	1	U_SEP1	Flash:32KB EEPROM:2KB
1U 8x2.5” Backplane				
SEP internal EEPROM	Non-Volatile	1	U_SEP1	Flash:32KB

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
				EEPROM:2KB
PERC for 1U 8x2.5”(H330 MM PERC)				
NVSRAM memory	Non-Volatile	1	U1033	128KB
FRU	Non-Volatile	1	U1019	256B
1-Wire EEPROM	Non-Volatile	1	U1004	128B
SBR	Non-Volatile	1	U1020	8KB
Flash	Non-Volatile	1	U3	16MB
1U 10x2.5” Backplane				
SEP internal EEPROM	Non-Volatile	1	U_SEP1	EEPROM: 2KB
SEP internal flash	Non-Volatile	1	U_SEP1	Flash:64kb
t FRU image	Non-Volatile	1	U27	EEPROM:8Kb
PERC for 1U 10x2.5”(H740P PERC)				
NVSRAM memory	Non-Volatile	1	U1087	128KB
FRU	Non-Volatile	1	U1019	256B
SPD	Non-Volatile	1	U22	256B
Flash	Non-Volatile	1	U1086	16MB
Backup Flash	Non-Volatile	1	U1100	8GB
SDRAM	Volatile	9	U1077-U1085	8GB
ACE IDSDM - vFlash				
vFlash (uSD)	Non-Volatile	1	J_Ace1	Nand Flash :16GB
iDSDM (uSD1, uSD2)	Non-Volatile	1	J_Ace1	Nand Flash :16GB,32GB,64GB
TPM				
Trusted Platform Module (TPM, TPM 2.0 only)	Non-Volatile	1	U_TPM	128 Bytes
Left (Quick Sync 2.0 module) Ear				
MCU	Non-Volatile	1	USAM7	32Mb
Left (status) Ear				
MCU	Non-Volatile	1	U_TINY	8KB

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Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
BOSS				
SPI Flash	Non-Volatile	1	U17	1024KB
TFRU	Non-Volatile	1	U7	64KB
LCD Bezel				
Microcontroller	Non-Volatile	1	IC1	256KB
Right Ear				
SPI Flash	Non-Volatile	1	U2	32Mb

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Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
Planer			
CPU Internal CMOS RAM	Battery-backed CMOS RAM	No	Real-time clock and BIOS configuration settings
BIOS SPI Flash	SPI Flash	Yes	Boot code, system configuration information, UEFI environment, Flash Disceptor, ME
iDRAC SPI Flash	SPI Flash	No	iDRAC Uboot (bootloader), server managent persistent store (i.e. IDRAC MAC Address, iDRAC boot variables), lifecycle log cache, virtual planar FRU and EPPID, rac log, System Event Log,
BMC EMMC	eMMC NAND Flash	No	Operational iDRAC FW, Lifecycle Controller (LC) USC partition, LC service diags, LC OS drivers, USC firmware
Memory VDDQ, CPU Vcore and VSA Regulators	OTP(one time programmable)	No	Operational parameters
System CPLD RAM	RAM	No	Not utilized
System Memory	RAM	Yes	System OS RAM
Trusted Platform Module (TPM, TPM 2.0 only)	EEPROM	Yes	Storage of encryption keys
Power Supplies			
Microcontroller	Flash PROM and EEPROM	Yes	Report PSU information and control firmware
1U 4x3.5” Backplane			
SEP internal flash	FLASH	NO	FW configuration data
SEP internal EEPROM	EEPROM	No	FRU
1U 8x2.5” Backplane			
SEP internal flash	Flash	No	FW configuration data
SEP internal EEPROM	EEPROM	No	FRU
PERC for 1U 8x2.5”(H330 MM PERC)			

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Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
NVSRAM memory	NVSRAM	No	Configuration data
FRU	FRU	No	Card manufacturing information
1-Wire EEPROM	1-Wire EEPROM	No	Holds default controller properties/settings
SBR	SBR	No	Boot loader
Flash	Flash	No	Card firmware
1U 10x2.5" Backplane			
Flash memory	Flash	No	Card firmware
BP FRU image	EEPROM	No	FRU
PERC for 1U 10x2.5"(H740P)			
NVSRAM memory	NVSRAM	No	Configuration data
FRU	FRU	No	Card manufacturing information
SPD	SPD	No	Memory configuration data
Flash	Flash	No	Card firmware
Backup Flash	Backup Flash	No	Holds cache data during power loss
SDRAM	SDRAM	No	Cache for HDD I/O
ACE IDSDM - vFlash			
vFlash (uSD)	NAND flash	Yes	Populate out-of-band or optionally connect to the host as mass storage and boot mechanism
iDSDM (uSD1, uSD2)	NAND flash	Yes	Provides mass storage
TPM			
Trusted Platform Module (TPM, TPM 2.0 only)	EEPROM	Yes	Storage of encryption keys
Left (Quick Sync 2.0 module) Ear			
MCU	embedded Flash	No	Card firmware
Left (status) Ear			

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Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
MCU	embedded Flash	No	Card firmware
BOSS			
SPI Flash	FLASH EEPROM	No	Boot code, FW
TFRU	FLASH EEPROM	Yes	Thermal monitoring
LCD Bezel			
Microcontroller	Internal Flash	No	Boot loader and s/w implementation of LCD command set
Right Ear			
SPI Flash	SPI Flash	No	For field maintenance. Have License, Service Tag and system information.

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Item	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
Planer			
CPU Internal CMOS RAM	BIOS	N/A – BIOS only control	1) Set NVRAM_CLR jumper to clear BIOS configuration settings at boot and reboot system. 2) Power off the system, remove coin cell battery for 30 seconds, replace battery and then power back on. 3) Restore default configuration in F2 system setup menu.
BIOS SPI Flash	SPI interface via iDRAC	Software write protected	Not possible with any utilities or applications and system is not functional if corrupted or removed.
BIOS Recovery SPI Flash	SPI interface via PCH	Software write protected	Not possible with any utilities or applications and the system is not functional if BIOS SPI is corrupted or removed.
iDRAC SPI Flash	SPI interface via iDRAC	Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed.	The user cannot clear memory completely. However, user data, lifecycle log and archive, SEL, and fw image repository can be cleared using Delete Configuration and Retire System, which can be accessed through the Lifecycle Controller interface.
BMC EMMC	NAND Flash interface via iDRAC	Embedded FW write protected	The user cannot clear memory completely. However, user data, lifecycle log and archive, SEL, and fw image repository can be cleared using Delete Configuration and Retire System, which can be accessed through the Lifecycle Controller interface.
Memory VDDQ, CPU Vcore and VSA Regulators	Once values are loaded into register space a cmd writes to nvm.	There are passwords for different sections of the register space	The user cannot clear memory.
System CPLD RAM	Not utilized	Not accessible	Not accessible
System Memory	System OS	OS Control	Reboot or power down system
Trusted Platform Module (TPM, TPM 2.0 only)	Using TPM Enabled operating systems	SW write protected	F2 Setup option
Power Supplies			
Microcontroller	The data is flash via Dell Update Package(DUP)	Using signature and manufacture key to protect memory write	Before firmware update, the memory will be clear.
1U 4x3.5” Backplane			
SEP internal flash	Pre-programmed before assembly	Not WP	The user cannot clear memory.

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Item	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
SEP internal flash	Programmed at ICT during production.	Not WP	The user cannot clear memory.
1U 8x2.5" Backplane			
SEP internal flash	Pre-programmed before assembly	Not WP	The user cannot clear memory.
SEP internal flash	Programmed at ICT during production.	Not WP	The user cannot clear memory.
PERC for 1U 8x2.5"(H330 MM PERC)			
NVSRAM memory	ROC writes configuration data to NVSRAM	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
FRU	Programmed at ICT during production.	Not WP	Cannot be cleared with existing tools available to the customer
1-Wire EEPROM	ROC writes data to this memory	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
SBR	Pre-programmed before assembly	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
Flash	Pre-programmed before assembly. Can be updated using Dell/LSI tools	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
1U 10x2.5" Backplane			
Flash memory	Pre-programmed before assembly. Can be updated using Dell/LSI tools	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
BP FRU image	Programmed at ICT during production.	Not WP	The user cannot clear memory.
PERC for 1U 10x2.5" (H740P)			
NVSRAM memory	ROC writes configuration data to NVSRAM	Not WP. Not visible to Host Processor	User cannot clear the memory.
FRU	Programmed at ICT during production.	Not WP	User cannot clear the memory.
SPD	Pre-programmed before assembly	Not WP. Not visible to Host Processor	User cannot clear the memory.
Flash	Pre-programmed before assembly. Can be updated using Dell/LSI tools	Not WP. Not visible to Host Processor	User cannot clear the memory.
Backup Flash	FPGA backs up DDR data to this device in case of a power failure	Not WP. Not visible to Host Processor	Flash can be cleared by powering up the card and allowing the controller to flush the contents to VDs. If the VDs are no longer available, cache can be cleared by going into controller BIOS and selecting Discard Preserved Cache.
SDRAM	ROC writes to this memory - using it as cache for data IO to HDDs	Not WP. Not visible to Host Processor	Cache can be cleared by powering off the card
ACE IDSDM - vFlash			
vFlash (uSD)	User can provide data to iDRAC (entirely in the iDRAC domain) to be pushed into vFlash	No write protect	1. The card may be physically removed and destroyed or cleared via standard means on a separate computer. Or 2. The user has access to the card in the host domain and may clear it manually.
iDSDM (uSD1, uSD2)	Device resides in host domain; they are exposed to the user via an internally connected, non-	Physical write protect switch on ACE card	(1) card may be physically removed and destroyed or cleared via standard means on a separate computer OR

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Item	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
	removable USB mass storage device		(2)User has access to the card in the host domain and may clear it manually
TPM			
Trusted Platform Module (TPM, TPM 2.0 only)	Using TPM Enabled operating systems	SW write protected	F2 Setup option
Left (Quick Sync 2.0 module) Ear			
MCU	Pre-programmed before assembly	N/A	The user cannot clear memory.
Left (status) Ear			
MCU	Pre-programmed before assembly	N/A	The user cannot clear memory.
BOSS			
SPI Flash	By programming the image via firmware update process	N/A	Use Flash tool, type “go.nsh w y”
TFRU	During Manufacturing, by programming the image via firmware update process. During runtime, by I2C Proprietary Command Protocol	N/A	By writing to Flash
LCD Bezel			
Microcontroller	Updated as part of secure iDRAC software update. Configuration parameters can change only as part of iDRAC update	Writes are only allowed as part of secure iDRAC update	not user clearable.
Right Ear			
SPI Flash	SPI interface via iDRAC	Hardware strapping	The user cannot clear memory.

NOTE: For any information that you may need, direct your questions to your Dell Marketing contact.

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